a second signal path coupled between said first memory array and said input/output circuit.

--30. A semiconductor integrated circuit device according to claim 29, further comprising:

a second memory array including a plurality of DRAM memory cells coupled to said logic circuit and said input/output circuit.

--31. A semiconductor integrated circuit device according to claim 29, wherein each of the plurality of DRAM memory cells includes a MOS transistor and a capacitor.

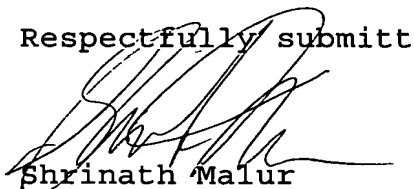
--32. A semiconductor integrated circuit device according to claim 30, wherein each of the plurality of DRAM memory cells includes a MOS transistor and a capacitor.--

REMARKS

New claims 26-32 have been added. No claims have been canceled or amended. Accordingly, claims 25-32 are currently pending in the application.

Examination is respectfully requested.

Respectfully submitted,



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Date: June 1, 2001